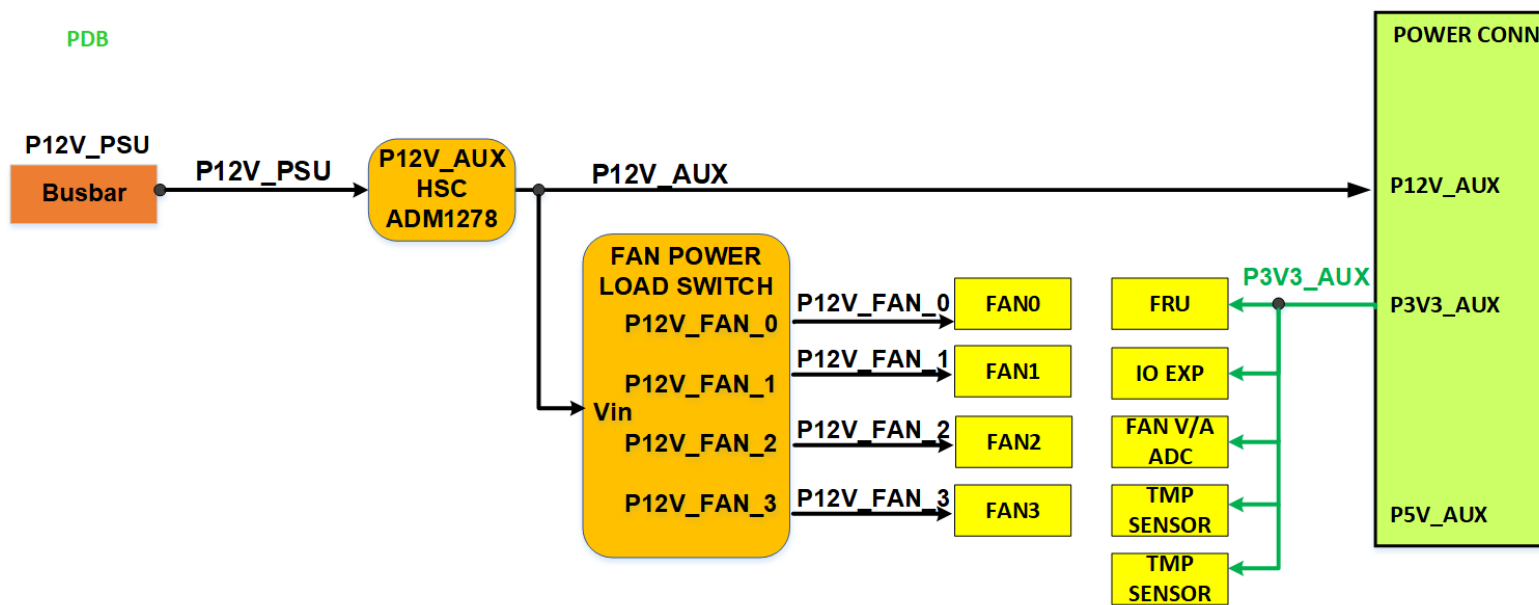


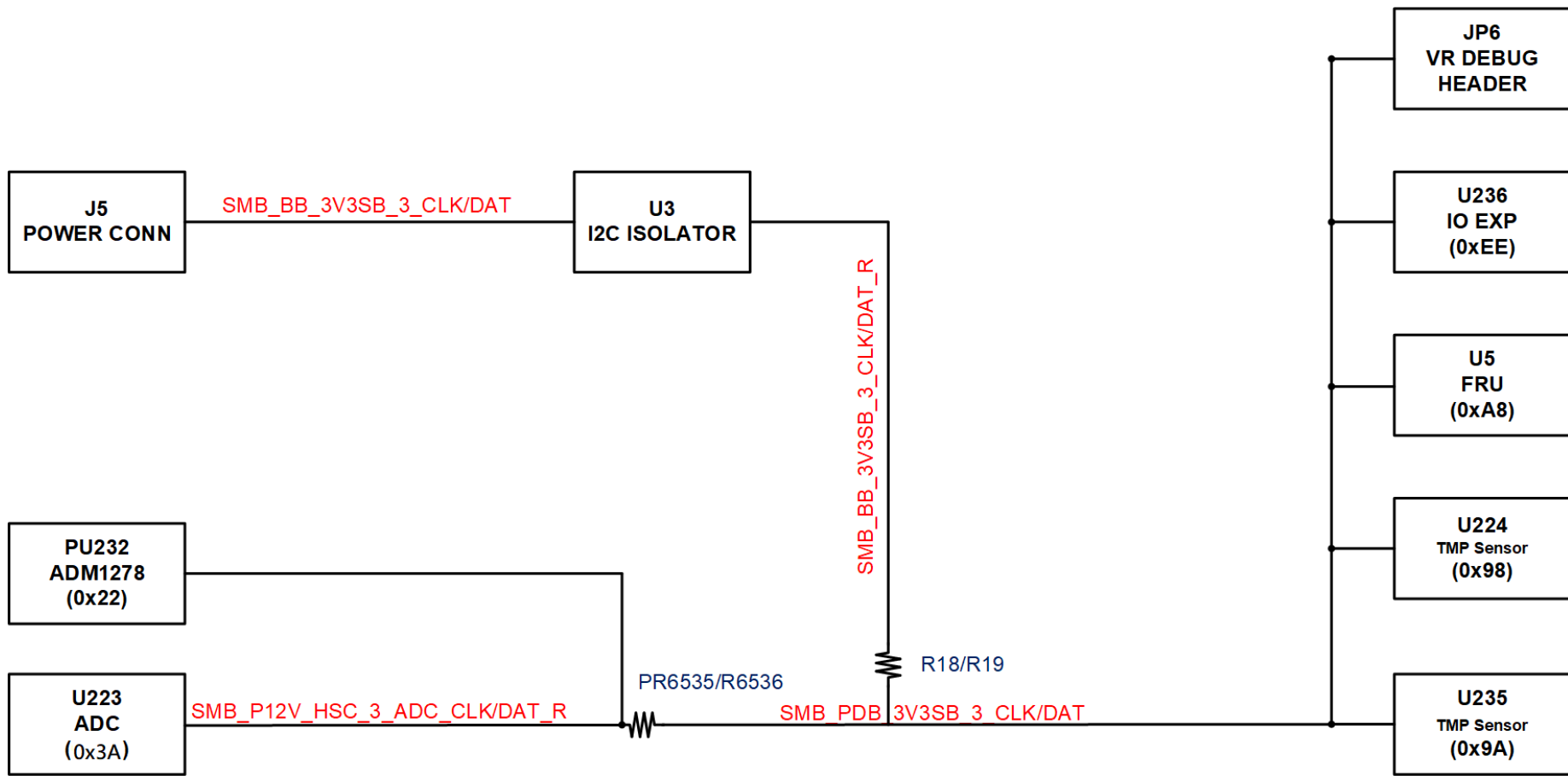
F0CE_PDB

Project Name : F0CE
PCB Number: DAF0CEPB8D0
PCB REV: D
PCBA REV: 35F0CPB0020
LAST UPDATE: 2020/12/15

INDEX

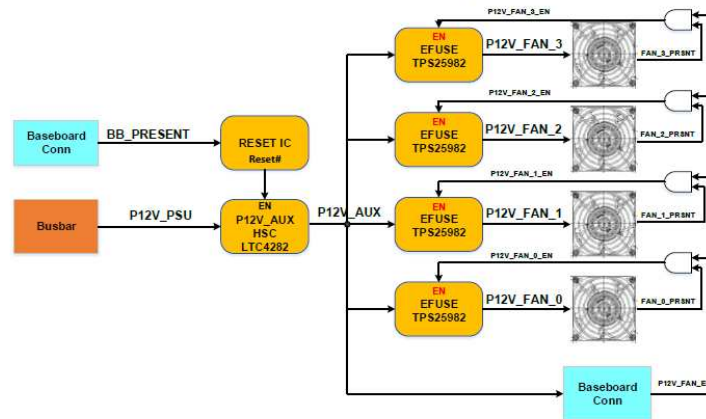
01	Cover Page	23	BLANK
02	Page Index	24	TO FAN MODULE CONN_1
03	BOARD BLOCK DIAGRAM	25	TO FAN MODULE CONN_1
04	I2C BLOCK DIAGRAM	26	TO BB CONN
05	POWER SEQUENCE DIAGRAM	27	BLANK
06	BUS BAR NUT	28	BLANK
07	BLANK	29	BLANK
08	I2C ISOLATION	30	HSC_P12V_AUX_1
09	TMP Sensor	31	P12V AUX HSC_2
10	FRU	32	P12V AUX HSC_3
11	BLANK	33	BLANK
12	IO EXP	34	BLANK
13	FAN PWM BUFFER_1	35	POWER GOOD LED
14	FAN PWM BUFFER_2	36	BLANK
15	FAN PRESENT BUFFER	37	FAN ENABLE
16	BLANK	38	EFUSE P12V_FAN
17	BLANK	39	VOLTAGE/CURRENT MON ADC
18	BLANK	40	GUIDE PIN & ME PART
19	PMBUS HSC ALERT BUFFER	41	SCREW HOLE
20	BLANK	42	LOSS COUPON
21	BLANK	43	Dummy Symbol
22	BLANK		





I2C BLOCK DIAGRAM

Power On/Off Sequence

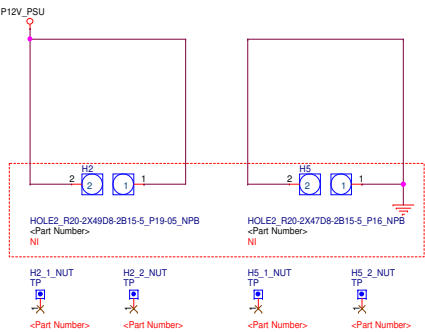


Power On

- ① P12V_PSU ON
- ② BB_PRESENT turn HIGH
- ③ RESET IC Delay 200 ms to Enable P12V_AUX HSC
- ④ Output P12V_AUX
- ⑤ P12V_FAN_EN turn HIGH
- ⑥ Output P12V_FAN

Power Off

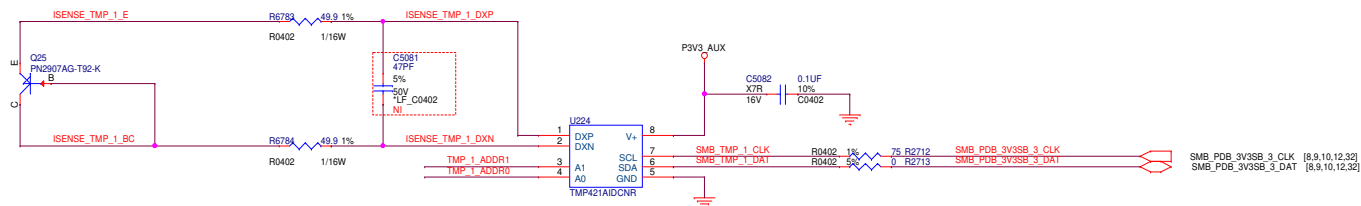
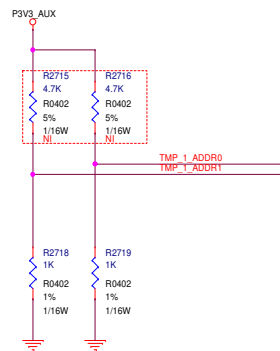
- ① P12V_PSU OFF
- ② BB_PRESENT turn LOW
- ③ RESET IC Disable P12V_AUX HSC
- ④ Power off P12V_AUX
- ⑤ Power off P12V_FAN



BLANK

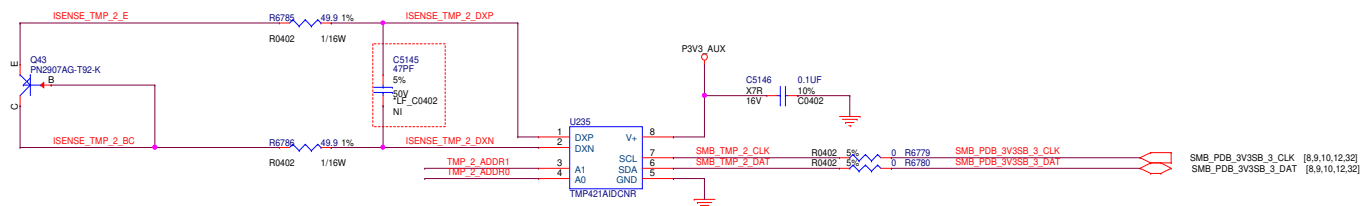
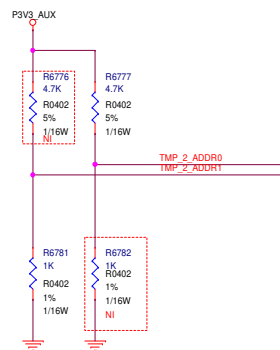
Q25_HOLDER

 TP
 <Part Number>



Q43_HOLDER

 TP
 <Part Number>



TWO-WIRE SLAVE ADDRESS	A1	A0
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

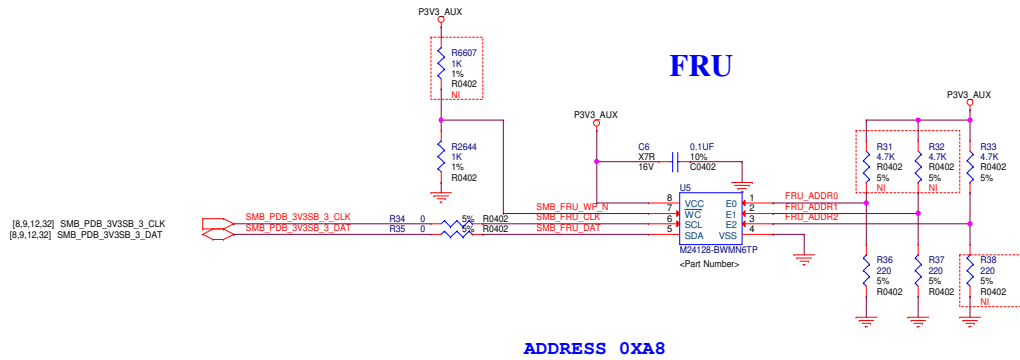


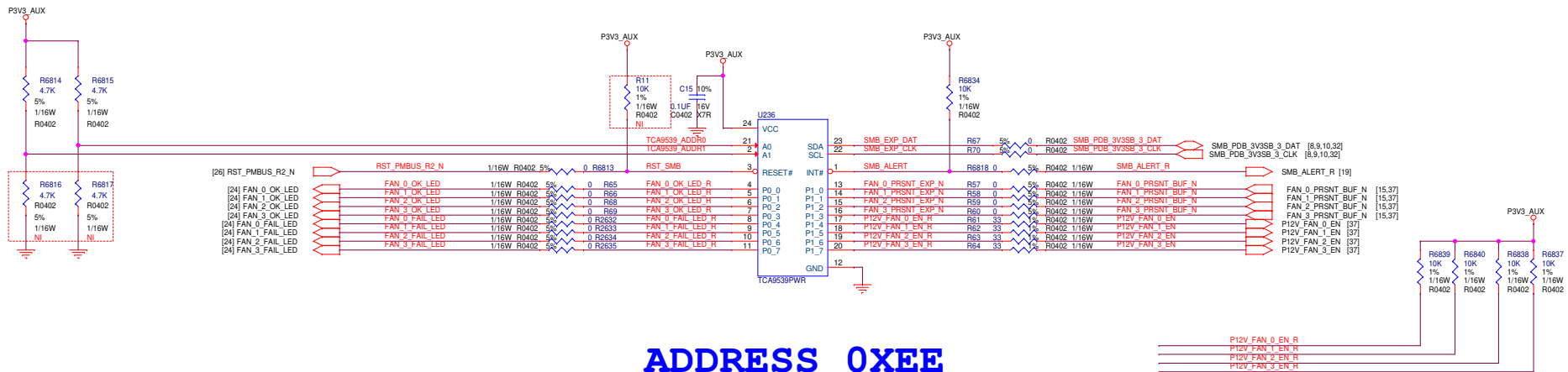
Table 2. Device Select Code

	Device Type Identifier ¹				Chip Enable Address ²			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	RW

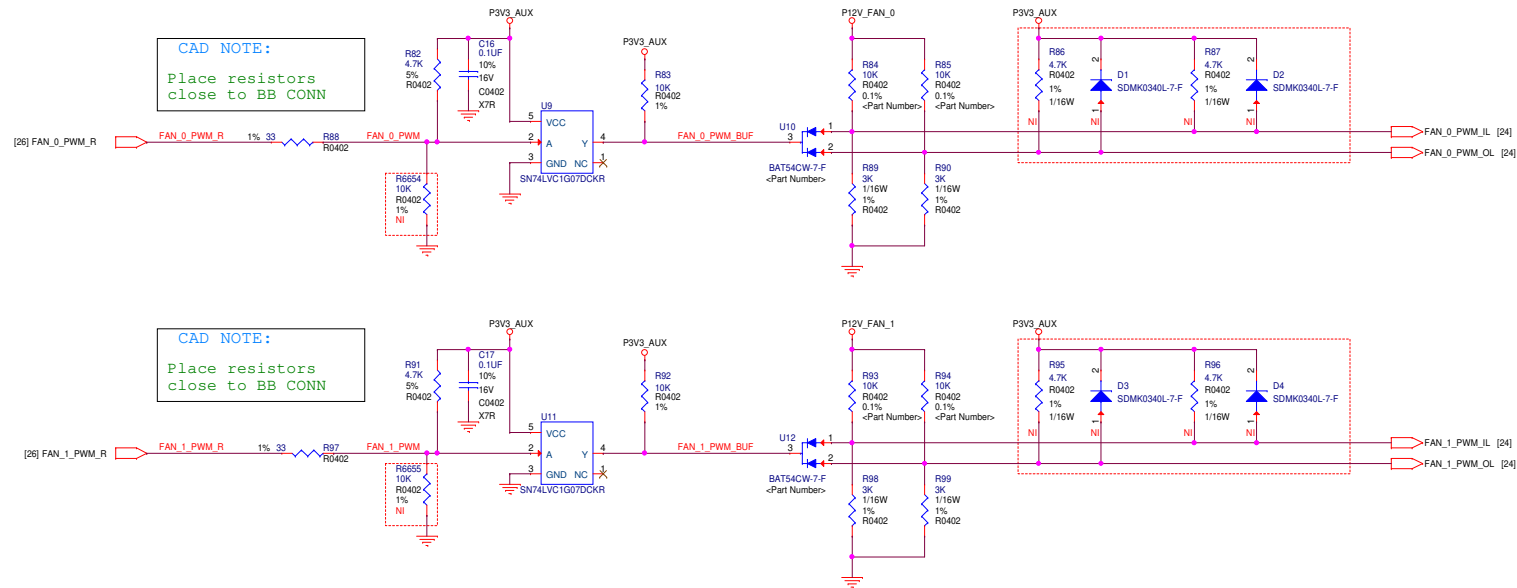
Note: 1. The most significant bit, b7, is sent first.
 2. E0, E1 and E2 are compared against the respective external pins on the memory device.

FRU address

BLANK

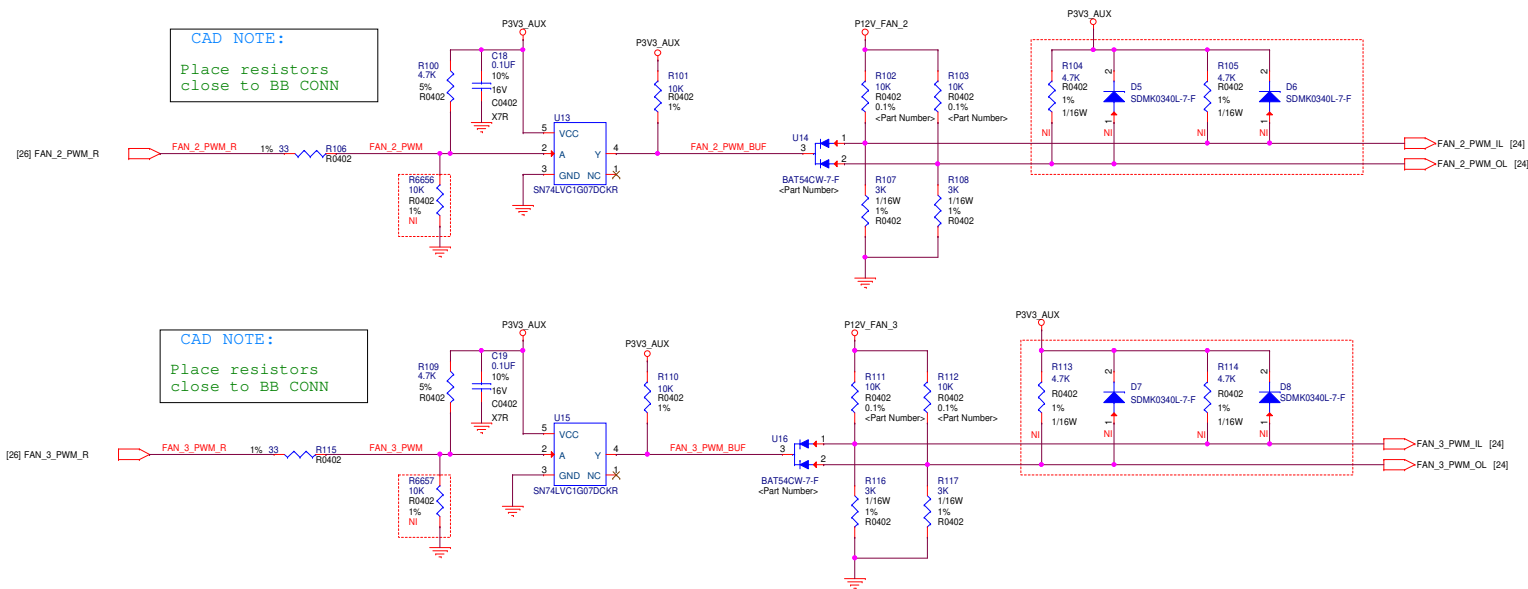


FAN 0&1 PWM BUFFER

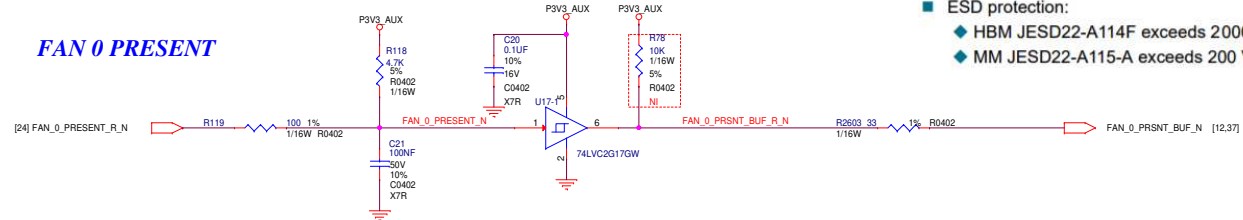


FAN PWM BUFFER_1

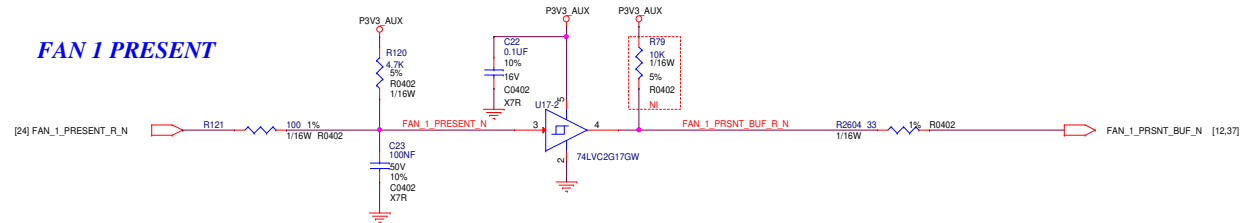
FAN 2&3 PWM BUFFER



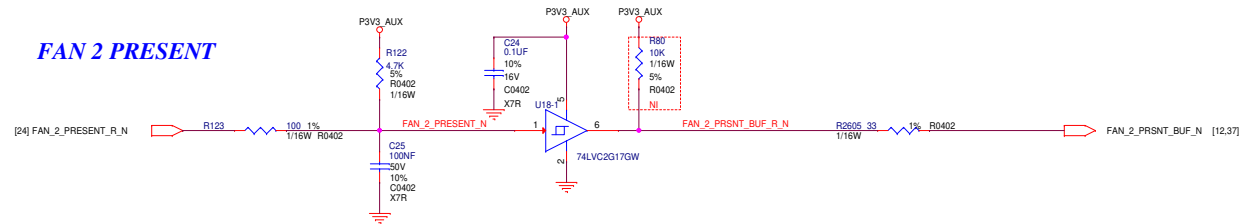
FAN 0 PRESENT



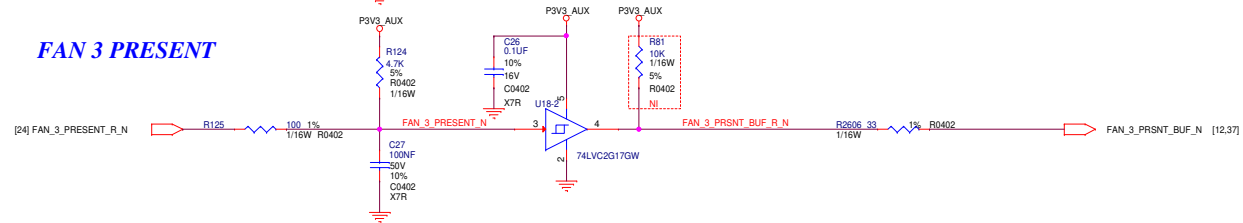
FAN 1 PRESENT



FAN 2 PRESENT



FAN 3 PRESENT



ESD protection:

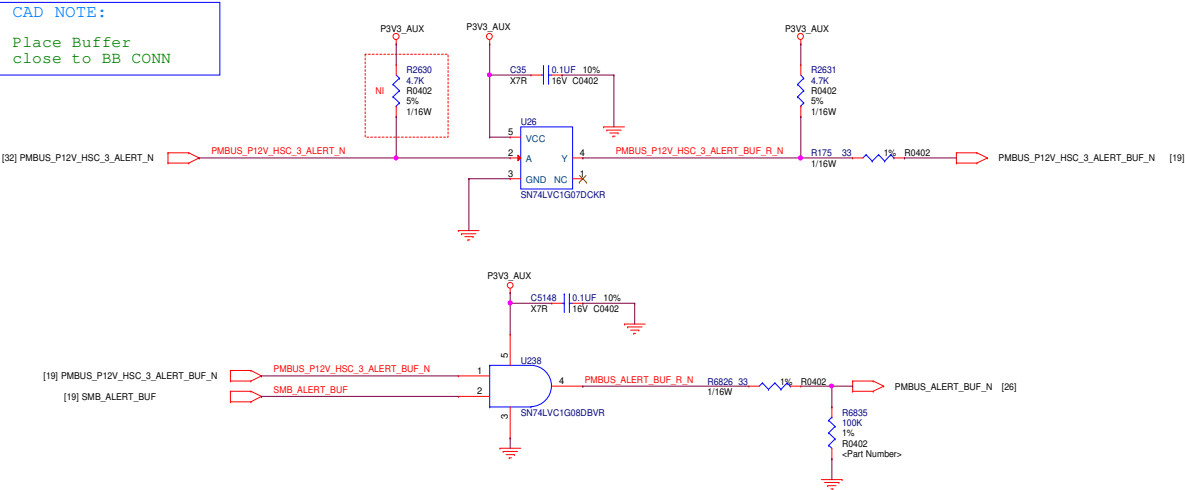
- ◆ HBM JESD22-A114F exceeds 2000 V
- ◆ MM JESD22-A115-A exceeds 200 V

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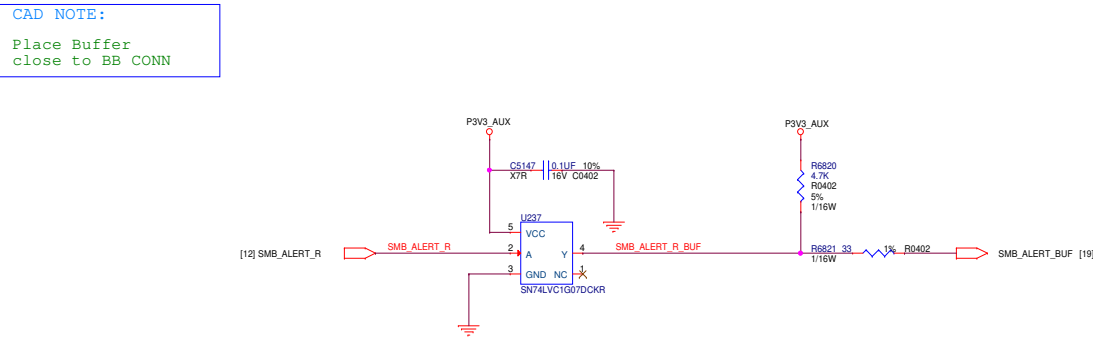
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P12V_AUX HSC ALERT



RST_PMBUS_ALERT

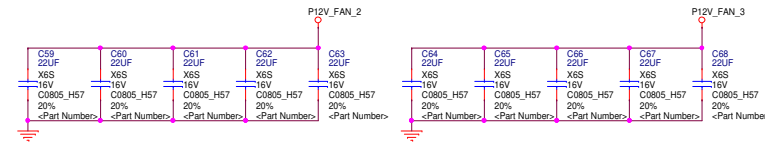


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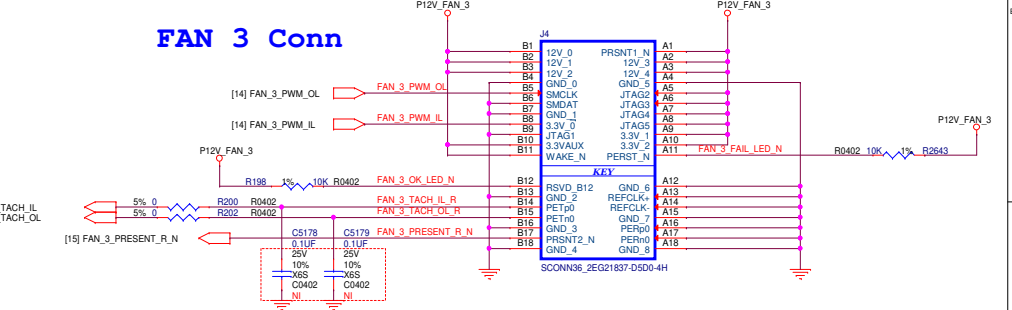
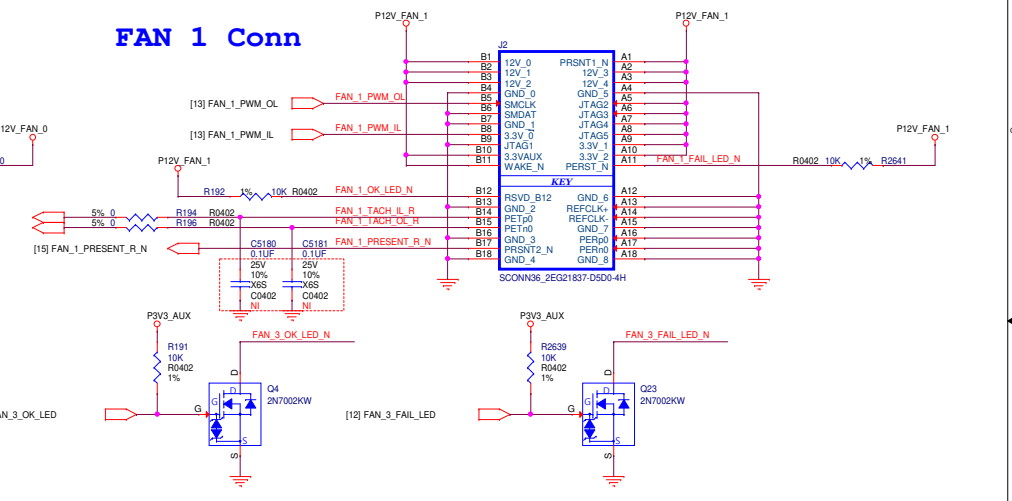
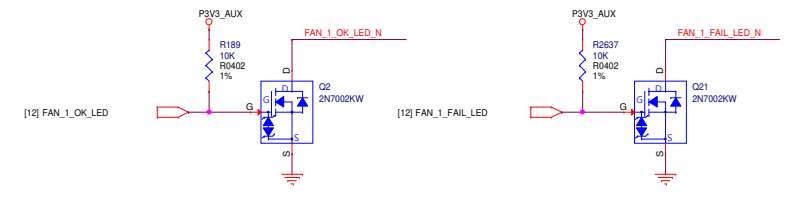
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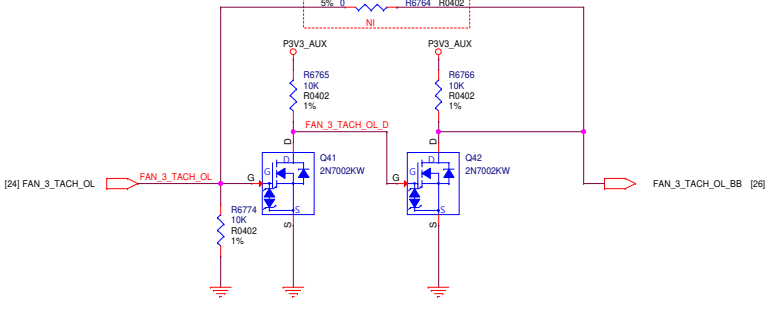
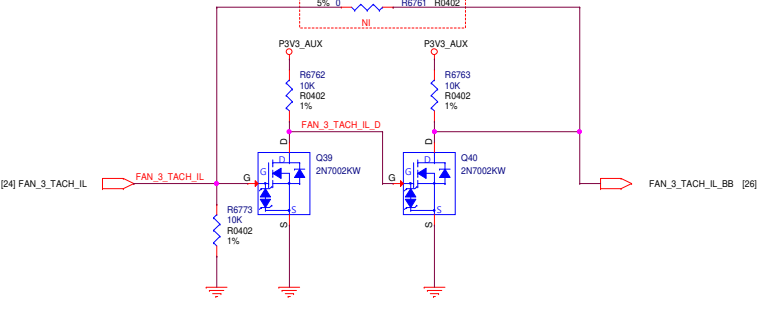
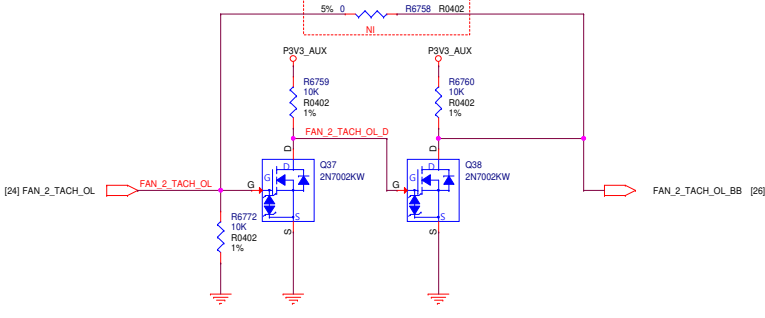
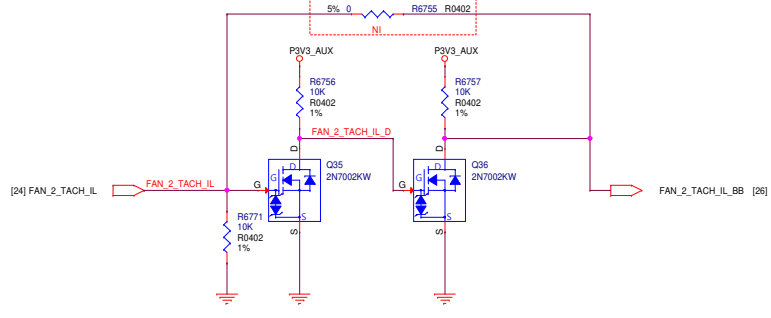
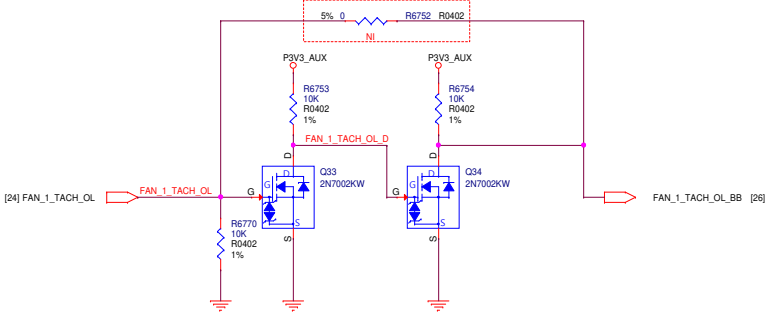
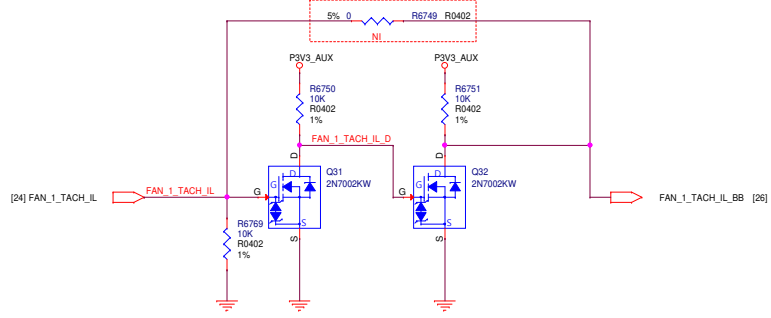
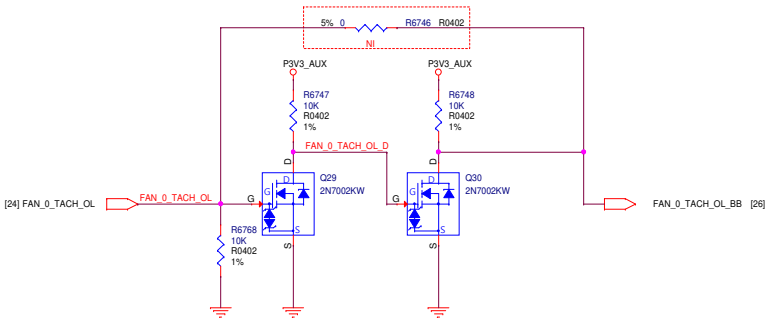
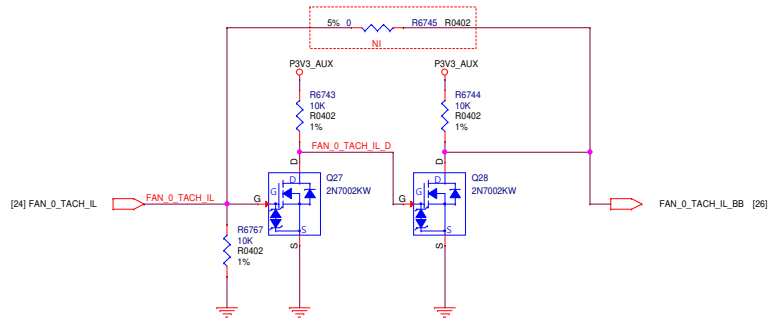


- Current Rating: 1.1A/PIN



FAN STATUS LED	FAN_0_STATE_LED_N	FAN_0_OK_LED_N	LED on FAN Module
FAN SPEED NORMAL	1	0	GREEN
FAN SPEED ABNORMAL	0	1	RED

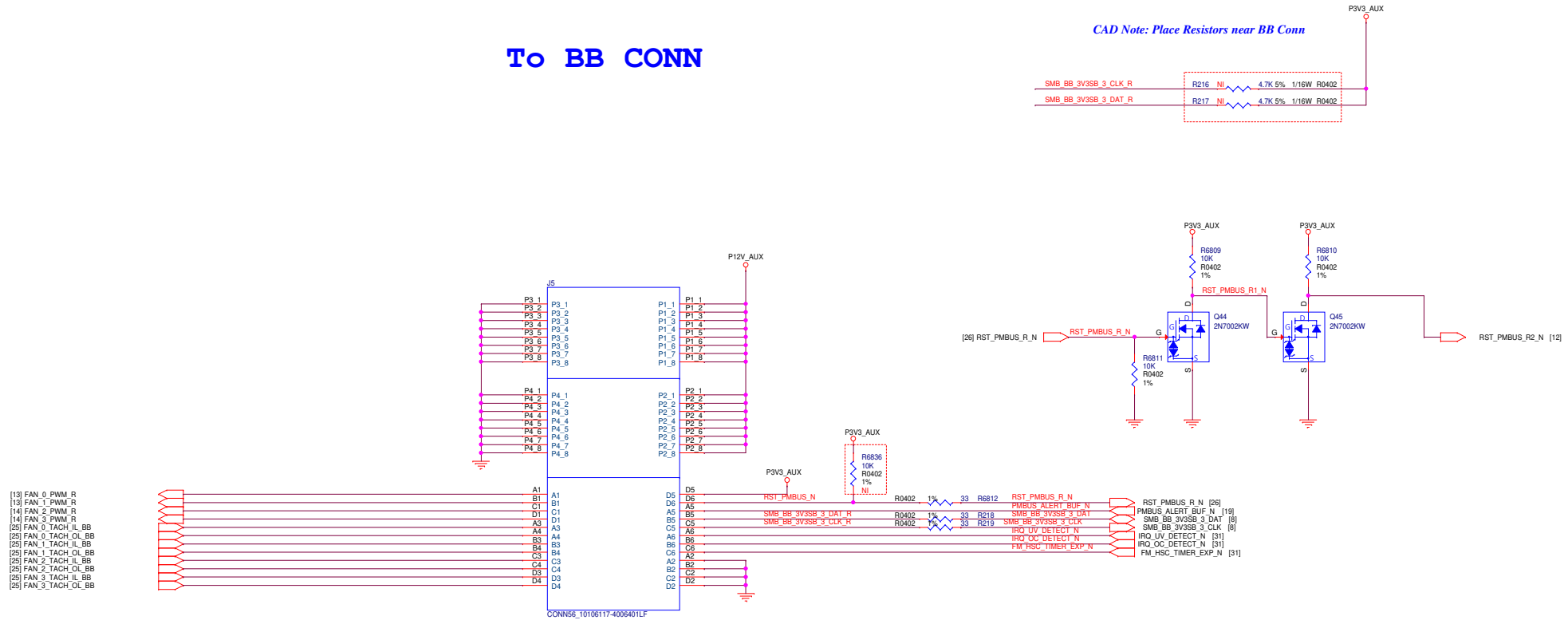
TO FAN MODULE CONN_1



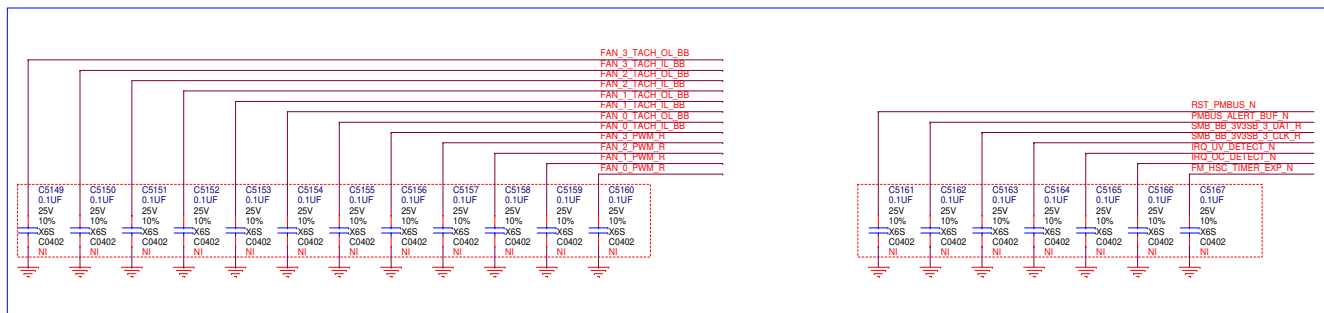
TO FAN MODULE CONN_2

To BB CONN

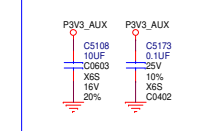
CAD Note: Place Resistors near BB Conn



CAD Note: Place CAP near BB Conn



CAD Note: Place CAP near BB Conn



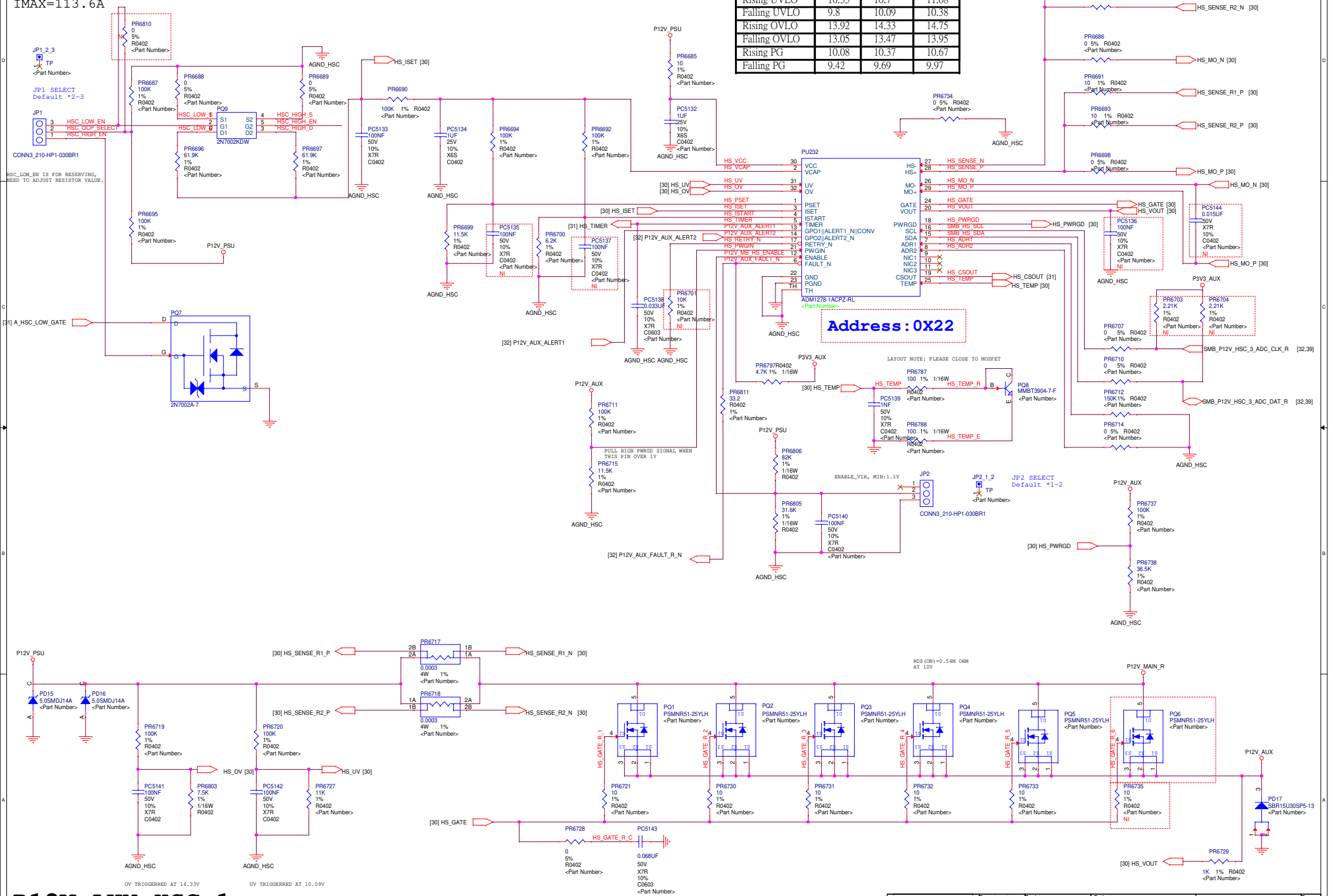
TO BB CONN

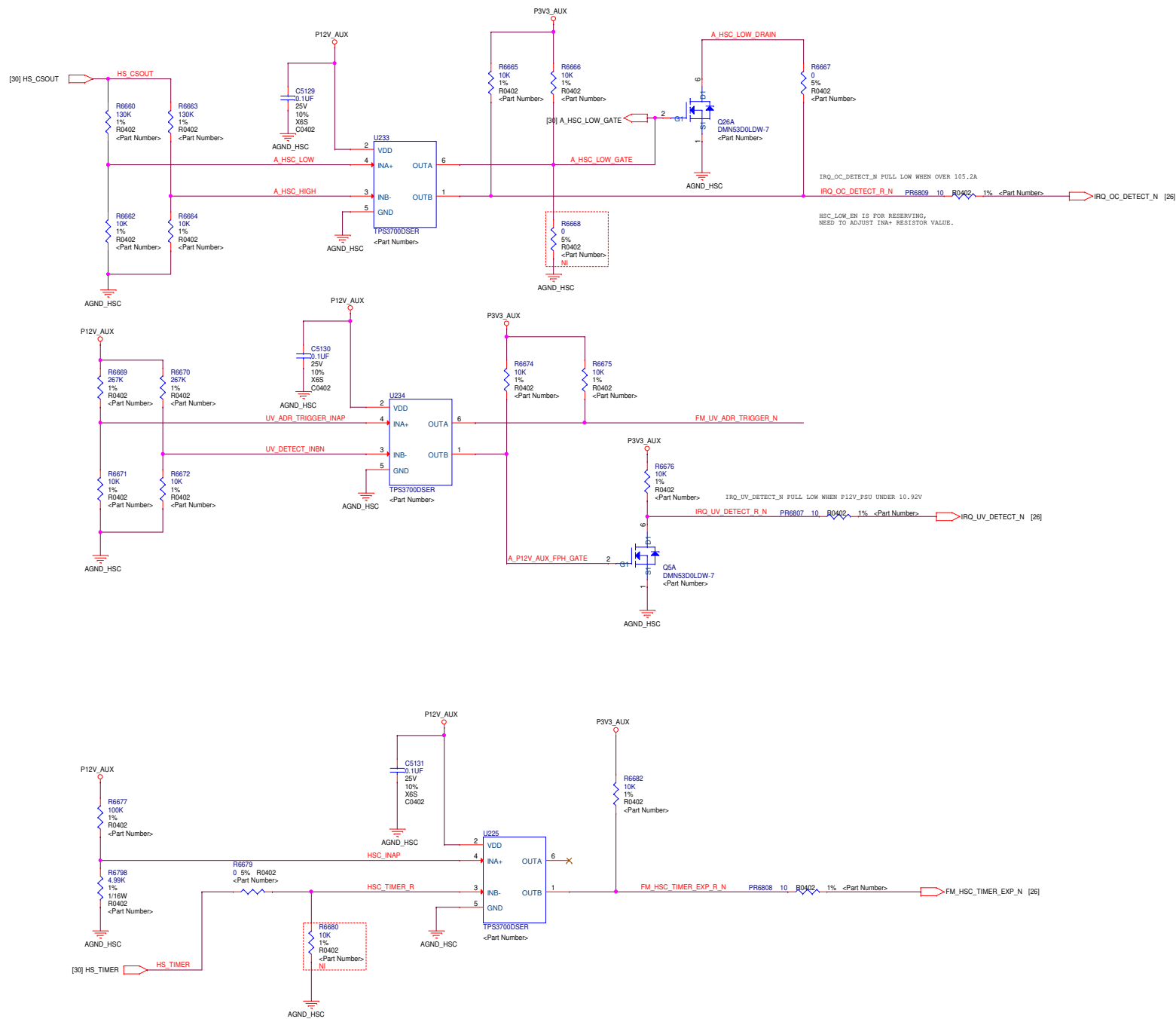
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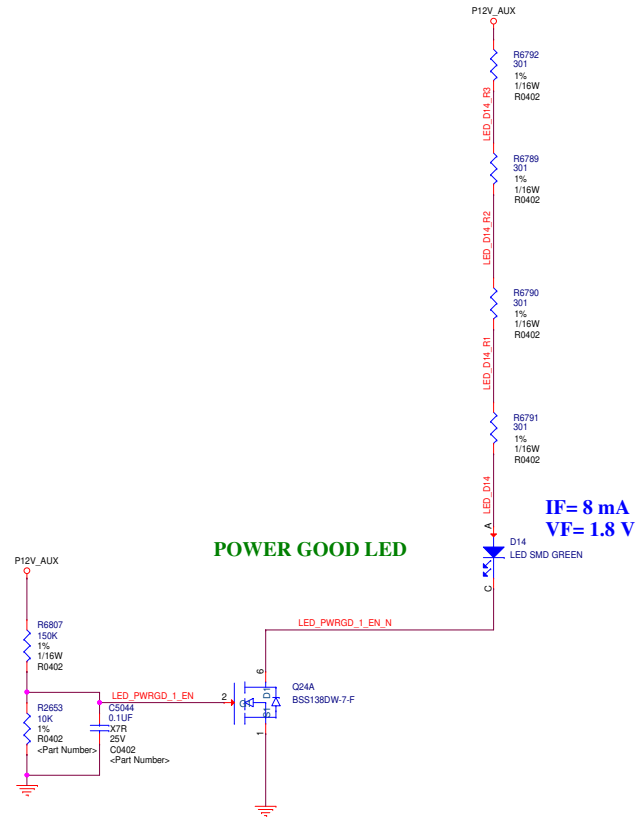
$I_{TRIP} = (V_{ISET} / 50) / R_{SENSE} = 126A$
 $V_{ISET} = 2.7V * (R_2 / (R_1 + R_2)) = 1.03V$
 $OCP = 126A$
 $TDC = 112.9A$
 $IMAX = 113.6A$





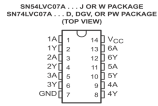
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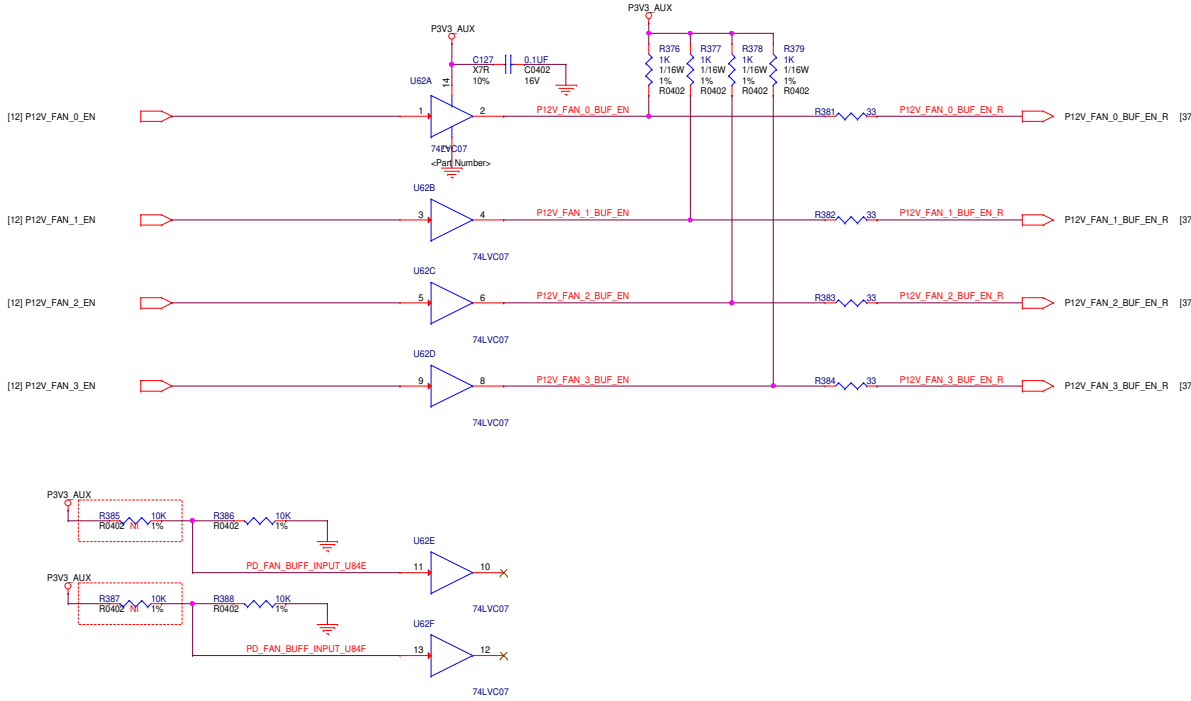
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U62 is positive open-drain buffer:



FUNCTION TABLE (each buffer/driver)	
INPUT A	OUTPUT Y
H	H
L	L

logic diagram, each buffer/driver (positive logic)



U54, U55, U60, U61 is inverse Schmitt-triggers:

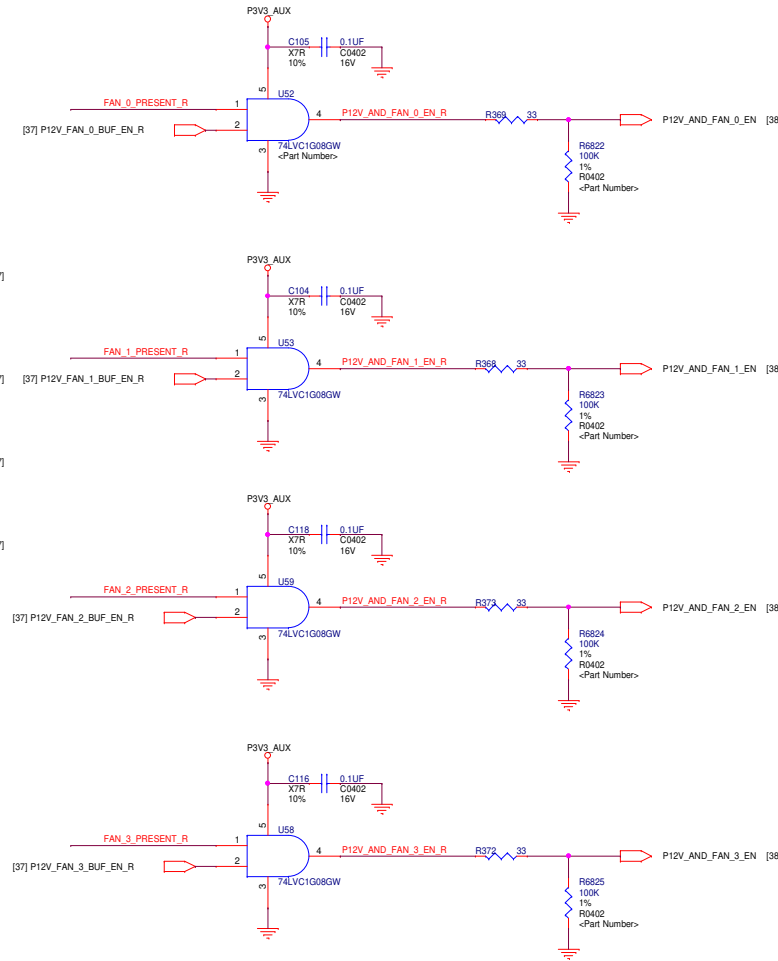
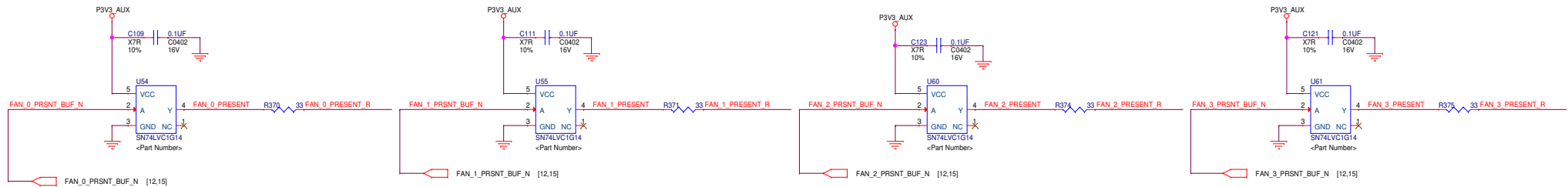
DBV OR DCK PACKAGE
(TOP VIEW)

FUNCTION TABLE	
INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

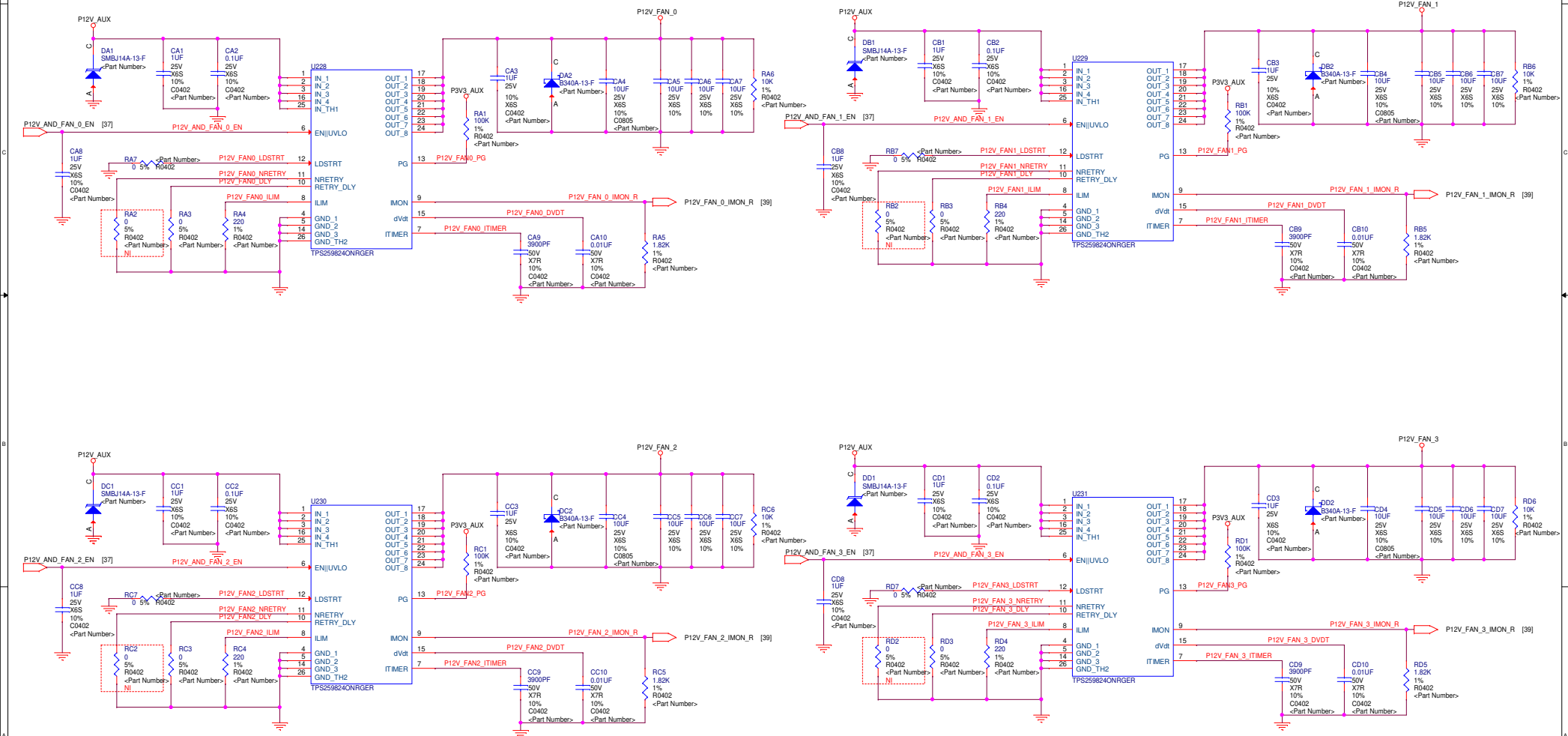


NC - No internal connection

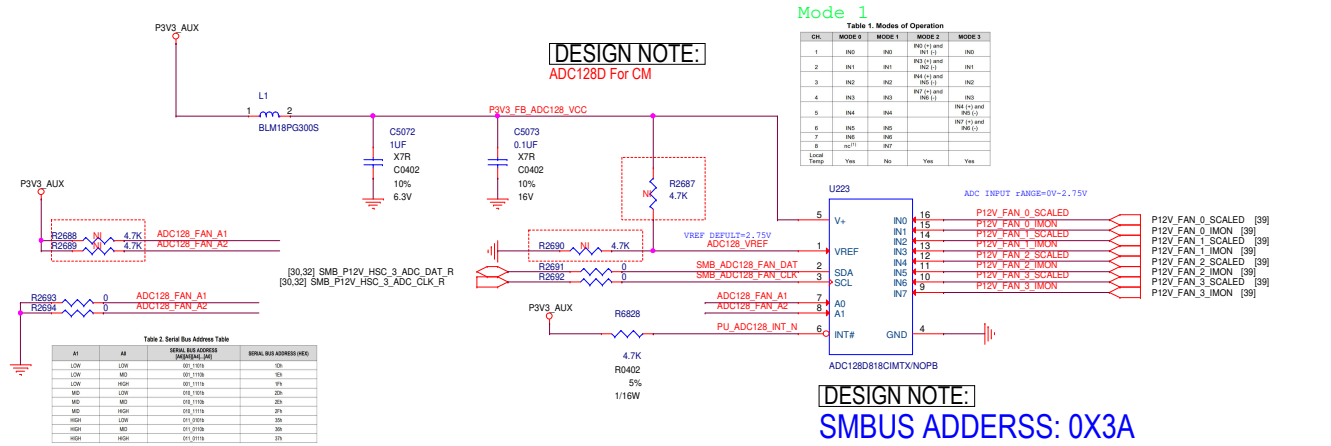


P12V_AUX Tolerance $\pm 10\%$ (10.8~13.2V)
Main mode=5A (max)
OCP= 6.75A

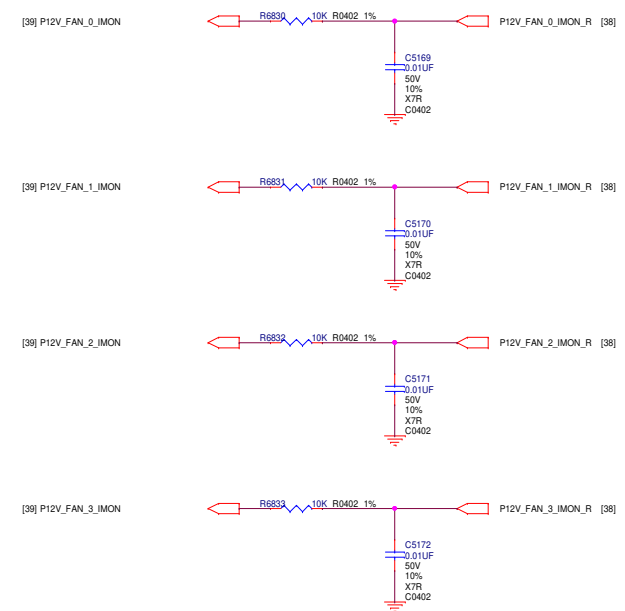
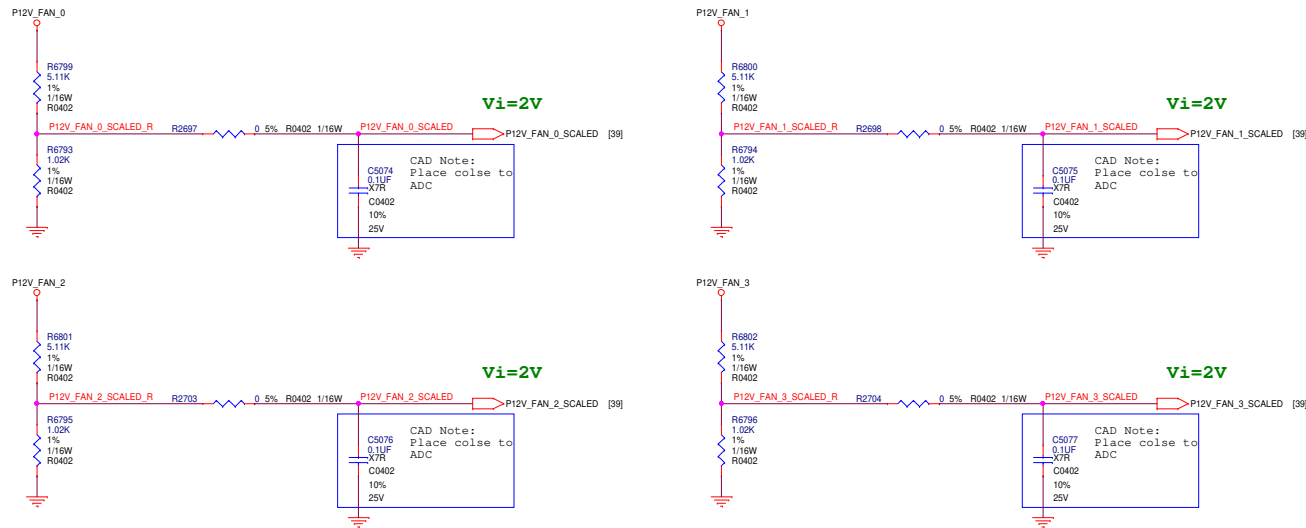
RETRY_DLY	NRETRY	DEVICE STATE
Short to GND	X	LATCH OFF
OPEN	open	4 auto-retries
OPEN	Short to GND	infinite number of retr



ROUTE ALL ADC NETS AT 10 MILLS WIDE



CAD Note: Place near ADC



THUMB SCREW*2



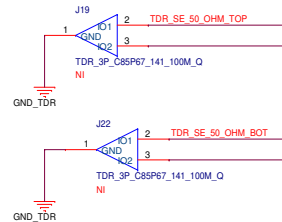
HADLE*2



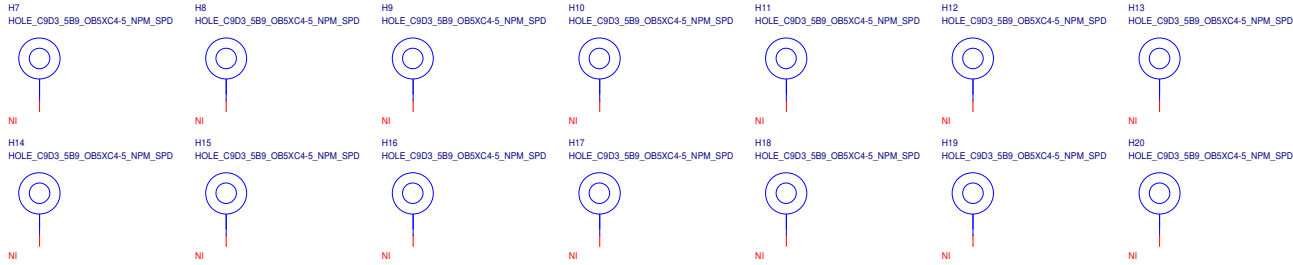
HANDLE SCREW*4



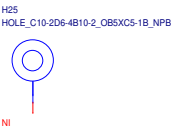
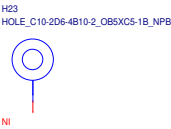
TDR



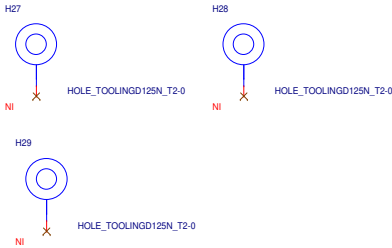
GOURD SCREW HOLE



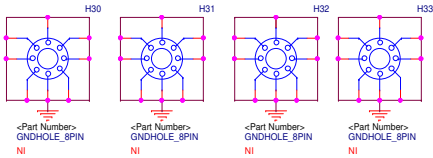
THUMB SCREW HOLE



Tooling Holes



HANDLE SCREW HOLE



[illegible]

PCBA_LABEL LABEL_SN_VPN_FBPn DUMMY_SYMBOL SNLABEL_27X6 <Part Number>	WEEE DMS DUMMY_SYMBOL WEEE NI	PB-E1 DM4 DUMMY_SYMBOL PB-ET_SMALL NI	BARCODE (TOP)	BARCODE (BOT)	
CE LOGO (TOP) DM10 DUMMY_SYMBOL CE_LOGO_5.8X5.08 NI	UL LOGO (TOP)	Quanta LOGO (TOP) DMS DUMMY_SYMBOL QUANTA_LOGO_7X26 NI	BMC AMI Laser label	PCB_VENDER_LOGO DMS DUMMY_SYMBOL PCB_VENDOR_LOGO_15X8 NI	
Dummy symbol					Quanta CCBU Department Designer Reviewer <Designer> <Reviewer> Project Size C Date: Tuesday, January 18, 2022 <Title> Page Title Sheet 43 of 43 Doc Number Page Title Sheet 43 of 43 Rev A